RCS32-E61AS

RCS32-E61AS Product appearance

Product Features

> Dedicated Type B Charging Pile Compatible with Onboard Type A6 Residual Current Protection Module
> All-in-One Highly Integrated Digital Residual Current Action Indicator
> Integrated Self-Test and Calibration Pins, Saving Customer Hardware Resources

Standard fit

> Complies with the residual current operating characteristic requirements for RDC-PD in Mode 3 charging according to GB/T 40820 (IEC 62955)
> Complies with the residual current operating characteristic requirements for RDC-MD in Mode 3 charging according to GB/T 40820 (IEC 62955)

XMD-Trip-Current (residual current related characteristics)

Wav.	Freq.	Min.	Typ.	Max.	Unit
2PDC	50Hz	4.0	5.0	7.0	mA
3PDC	50Hz	4.0	4.6	6.0	mA
S-DC	-	4.0	4.6	6.0	mA

XPD-Trip-Current (residual current related characteristics)

Wav.	Freq.	Min.	Typ.	Max.	Unit
AC	50Hz	21.0	23.2	26.0	mA
2PDC	50Hz	4.0	5.0	7.0	mA
3PDC	50Hz	4.0	4.6	6.0	mA
S-DC	-	4.0	4.6	6.0	mA

XMD-Trip-Time (residual current related characteristics)

Wav.	Current	Typ.	Max.	Unit
2PDC	60mA	50.0	100.0	ms
2PDC	200mA	50.0	300.0	ms
3PDC	60mA	50.0	100.0	ms
3PDC	200mA	50.0	300.0	ms
S-DC	6mA	120.0	10000.0	ms
S-DC	60mA	50.0	300.0	ms
S-DC	200mA	50.0	100.0	ms

XPD-Trip-Time (residual current related characteristics)

Wav.	Freq.	Current	Typ.	Unit
AC	50Hz	30mA	120.0	ms
AC	50Hz	60mA	50.0	ms
AC	50Hz	150mA	15.0	ms
AC	50Hz	5000mA	8.5	ms
A0	50Hz	42mA	110.0	ms
A0	50Hz	84mA	25.0	ms
A0	50Hz	350mA	10.0	ms
A0	50Hz	42mA+6mADC	45.0	ms
A0	50Hz	84mA+6mADC	20.0	ms
A0	50Hz	210mA+6mADC	15.0	ms
2PDC/3PDC	50Hz	60mA	40.0	ms
2PDC/3PDC	50Hz	120mA	15.0	ms
2PDC/3PDC	50Hz	300mA	15.0	ms
2PDC/3PDC	50Hz	5~50A	15.0	ms
S-DC	-	6mA	140.0	ms
S-DC	-	60mA	45.0	ms
S-DC	-	300mA	8.5	ms

XMD-NO Trip-Time (residual current related characteristics)

Wav.	Freq.	Current	Min.	Max.	Unit
AC	50Hz	30mA	-	-	ms
AC	50Hz	60mA	-	300	ms
AC	50Hz	150mA	-	80	ms
AC	50Hz	5A	>80	80	ms

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Electrical & Reliability Characteristics

Char.	Value
Working Temperature	-40℃~105℃
Storage Temparature	-40℃~105℃
Working humidity	≤95%
Supply Voltage（VDD） (1)	4.85~5.15 VDC
Consumption	≤110 mW
Voltage Input, low level	0~0.6VDC
Voltage Input, high level	4.2~5VDC
FIT (2)	Contact us
Designed Life (3)	≥ 20 years
Working Altitude (4)	≤ 4000m

(1) It is sugguested to control VDD within 4.9~5.1 VDC to get better performance

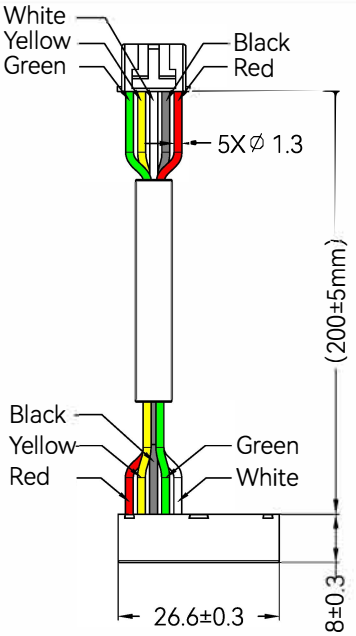
(2) The calculation of FIT according to IEC 61709 , is based on the FIT values of different different components in the BoM list . And the calculation principle : ground mobile , no dust or harmful substances

(3) The calculation and claim of product life is based on the MTBFvalue according to IEC 61709

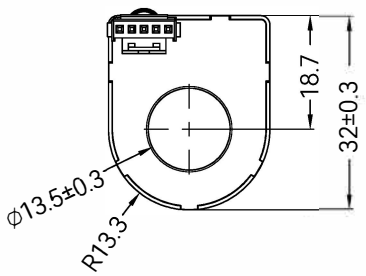
(4) The calculation about altitude is based on the principles :reinforced insulation , insulation material group III , pollution degree II ,overvoltage category II

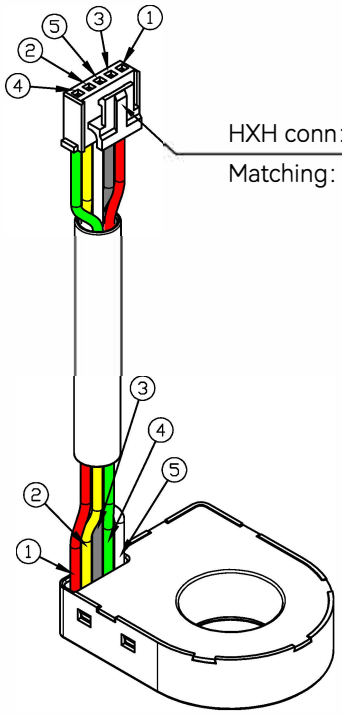
Mechanical dimensions

Top view



Rear view





3D simulation

HXH conn: HX20020-5P(HY)

Matching: HX20020-A
(HY/SMW200-A)

1: VDD（Red Line）
2: PD-OUT（Yellow Line）
3: GND（Black Line）
4: MD-OUT（Green Line）
5: TEST-IN（White Line）

* The limit deviation of unmarked dimensional tolerance shall be in accordance with GB/T 14486-MT5/B

Dimensions in mm

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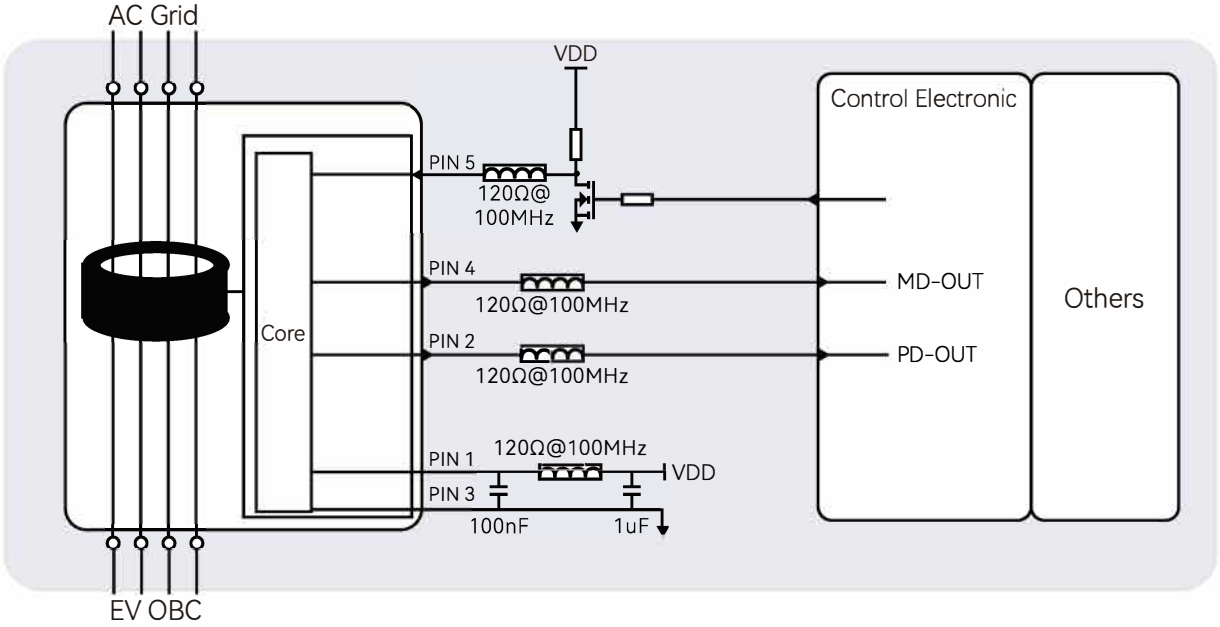
Typical Application Schematic & Pin Definition



Pin-No.	Pin Name	Function
PIN-1	VDD	> Product power supply pin, standard supply voltage 5 VDC > Input voltage range requires 4.85~5.15 VDC, power output capability > 100mA > Power ripple ≤ 150mV (LDO circuit recommended, special attention should be paid to the load response performance of the LDO chip, refer to power chip LP2985A-50DB) > It is recommended to add a ferrite bead to the PIN and place it close to the pin
PIN-2	PD-OUT	> If the residual current exceeds the preset trip value (for this module, usually 4.6 mADC or 22.5 mAAC), this output is in a high-level state (including during self-test) > Under other conditions, this output is in a low-level state (GND) > It is recommended to add a ferrite bead to the PIN and place it close to the pin
PIN-3	GND	> Product power ground pin
PIN-4	MD-OUT	> If the residual current exceeds the preset DC trip value (for this module, usually 4.6 mADC), this output is in a high-level state (including during self-test) > Under other conditions, this output is in a low-level state (GND) > It is recommended to add a ferrite bead to the PIN and place it close to the pin
PIN-5	TEST-IN	> When this pin is pulled low to 0 VDC, the system will detect the offset value of the current set zero point and store it in the MCU register to complete calibration > After calibration is completed, the system will internally generate a simulated residual current to test whether the module can respond correctly. During this process, if the module works properly, MD-OUT and PD-OUT will become high-level > It is recommended to add a ferrite bead to the PIN and place it close to the pin Note: > When using the TEST-IN function, the main circuit must be disconnected to ensure no residual current exists in the line, preventing abnormal calibration values for the product > When using this pin, please follow the recommended practical logic design

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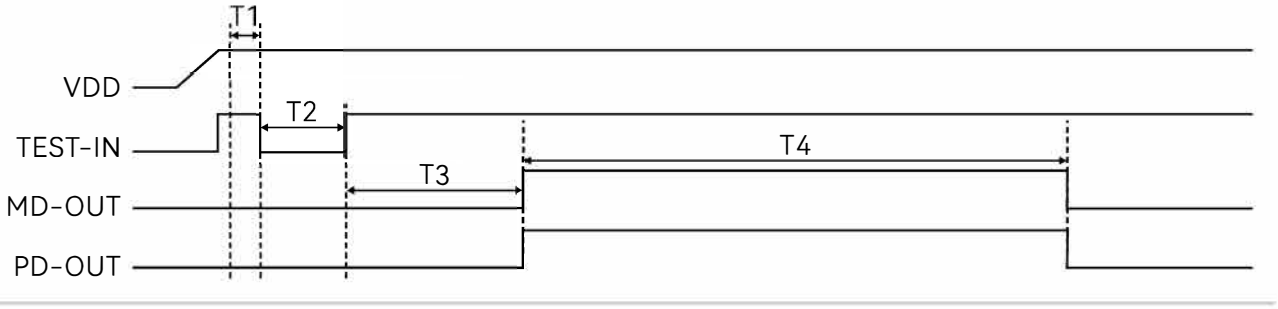
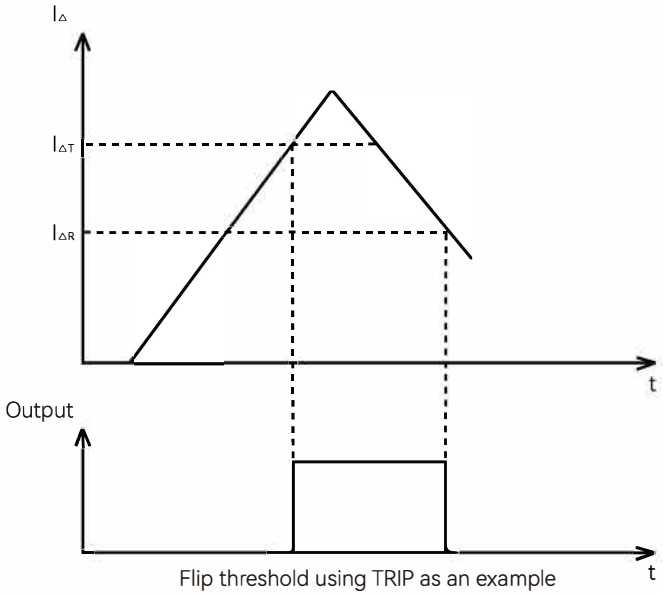
Timing Diagram



> It is recommended that VDD starts from 0V, with a monotonic power-up process lasting less than 15ms.
> T1 is the wait time after power-up is completed; it is recommended that T1 ≥ 100ms.
> T2 is the time for system self-check and internal calibration commands; it is recommended that 50ms ≤ T2 ≤ 1200ms. When the pin is at a low level for more than 50ms, the product begins self-check testing.
> T3 is the action signal delay time, T3 ≈ 280ms. It is recommended to detect the action signal 100ms after T5 ends.
> T4 is the action signal maintenance time after self-check is completed, T4 ≈ 1.5s. It is recommended to detect the action signal 100ms after T4 ends.

Note: During the self-check and calibration process (i.e., during T1, T2, T3, T4), do not close the main circuit switch to prevent residual current in the circuit from affecting the self-check and calibration process. Once the TRIP pin group inversion is finally received, it can be used to determine whether the RCD module is functioning normally for subsequent operations.

Digital Signal Flip Threshold



Flip threshold using TRIP as an example

> To minimize the jitter of digital signal output caused by instability of residual current, the digital logic output pins of the product are designed with a flip threshold setting.
> When the $I_{\triangle T}$ reaches the trip threshold, the TRIP pin flips; when the residual current decreases to $I_{\triangle R}$, the recovery threshold, the TRIP pin flips again to return to the normal state.
> The $I_{\triangle T}$ setting value is 100% of the typical action value, and the I△R setting value is 55% of the typical action value.

Version history

Version number	Modifications	Reason for modification
V0.1.0	The official version is released	
V0.1.1	Update product dimension drawings	Errata
V0.2.0	The UI of the product specification has been upgraded	
V0.2.1	Product Parameters and Typical Application Diagram Update	Errata
V0.2.2	Updated 3D Product Images and Dimension Drawings	Update